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Low Power Explicit Pulse Triggered Flip-Flop Design Based On A Pass Transistor

Amruta S. Vibhandik, Prof. P. V. Baviskar, Prof. K.N. Pawar

Abstract— *In VLSI system design, power consumption is the ambitious issue for the past respective years. Advanced IC fabrication technology grants the use of nano scaled devices, so the power dissipation becomes major problem in the designing of VLSI chips. In this paper we present, a low-power flip-flop (FF) design featuring an explicit type pulse-triggered structure and a modified true single phase clock latch based on a signal feed-through scheme using pass transistor. The offered design successfully figure out the long discharging path problem in conventional explicit type pulse-triggered FF (P-FF) designs and achieves better power performance by consuming low power. The proposed design also significantly reduces delay time, set-up time and hold time. Simulation results based on TMC 180nm CMOS technology reveal that the proposed design features the best power and delay performance in several FF designs under comparison.*

Keywords—Flip-Flop, low power consumption, pulse triggered, high-speed.

I. INTRODUCTION

Flipflops are the memory element of sequential circuit. Flip-flop are the basic storage elements that stores logical state of one or more input data signals in response to a clock pulse. They are fundamental building blocks of electronic system used extensively in all kinds of digital designs. Most digital designs nowadays often adopt intensive pipelining techniques and hire many flip-flop rich modules such as register file, shift register. Flip-flop is one of the most power consuming element in VLSI system. Generally it accounts 30%-60% of the total power dissipation in a system. So that it is necessary to work with such a flip-flop which consumes less power in overall system design [1], [2].

There are primarily two types of flip-flop. First one is the conventional flip-flop and another one is the pulse triggered flip-flop. Conventional flip-flop consist of two stages, one is the master and another one is slave. Master is activated when positive edge is triggered and slave is activated when negative edge is triggered. Conventional flip-flop such as master-slave flip-flop, sense amplifier based flip-flop are characterized by their hard edge property positive set-up time which causes. Large D-to-Q delay. On the other hand, Pulse-triggered FF (P-FF), because of its single-latch structure, is more popular than the conventional master–slave based FFs in high-speed applications. Besides the speed advantage, its simple circuitry is also beneficial to lowering the power consumption of the overall system. Pulse triggered flip-flop are characterized by their soft edge property negative set-up time which reduces D-to-Q delay. A P-FF which reduces two stages of conventional flip-flop into one stage, consists of a pulse generator for strobe signals and a latch for data storage. Since only one latch is needed, a P-FF is simpler in circuit complexity. This allows higher toggle rate for high-speed operations [3]–[8].

Depending on the method of pulse generation, pulse triggered flip-flop can be classified as implicit or explicit P-FF. In an implicit P-FF, the pulse generator is the part of the latch design and pulse signals are generate inside the flip-flop. In an explicit P-FF, pulse generator and latch are separate. Pulse signals are externally generate in the explicit P-FF. In this brief, we present a novel low-power explicit P-FF design based on a pass transistor. Observing the delay discrepancy in latching data “1” and “0,” the design reduces longer delay time by feeding the input signal directly to an internal node of the latch design to speed up the data transition. This is done by introducing a simple pass transistor for extra signal driving. When it is combined with the pulse generator, it forms a new P-FF design with increased speed performance Flip-flops are the memory element of sequential circuit. Flip-flop are the basic storage elements that stores logical state of one or more input data signals in response to a clock pulse. They are fundamental building blocks of electronic system used extensively in all kinds of digital designs. Most digital designs nowadays often adopt intensive pipelining techniques and employ many flip-flop rich modules such as register file, shift register. Flip-flop is one of the most power consuming element in VLSI system. Generally it accounts 30%-60% of the total power dissipation in a system. So that it is necessary to work with such a flip-flop which consumes less power in overall system design [1], [2].

II. LITERATURE SURVEY

H. Kawaguchi and Takayasu Sakurai worked on - A Reduced Clock-Swing Flip-Flop (RCSFF) for 63% Power Reduction [1] in May 1998. He proposed a reduced clock swing flip-flop (RCSFF) which is composed of a reduced swing clock driver with a special extra flip-flop which personifies current cut-off mechanism. The RCSFF can reduce one-third clock system power as compared to the other traditional flip-flops. This power improvement is obtained by reducing clock the swing down to 1V. Fabian

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Klass, Ashutosh Das and Gin Yee worked on - A New Family of Semi dynamic and Dynamic Flip-Flops with Embedded Logic for High-Performance Processors [2] in May 1999 to introduce a new family of semidynamic and dynamic edge triggered flip-flops which are compatible for high performance microprocessor design. James Tschanz, Siva Narendra, Vivek De, Zhanping Chen, Shekhar Borkar and Manoj Sachdev worked on - Comparative Delay and Energy of Single Edge-Triggered & Dual Edge-Triggered Pulsed Flip-Flops for High Performance Microprocessors [3] in May 2001. In this paper, different types of single edge-triggered flip flops, including static and semi dynamic along with both explicit as well as implicit pulse generation, are compared and studied. Bai-Sun Kong, Young-Hyun Jun and Sam-Soo Kim have worked on Conditional- Capture Flip-Flop (CDFF) for Statistical Power Reduction [4] in Aug 2001 to prove that the proposed design attains power reduction by eliminating redundant transitions of internal nodes. This paper provides the analysis of conventional high-performance flip-flops such as transmission-gate flip-flops (TGFFs), hybrid latch-flip-flops (HLFFs), semi-dynamic flip-flops (SDFFs), and sense amplifier-based flip-flops (SAFFs). The simulation results of this paper indicates that the proposed Conditional-Capture flip-flop achieves power savings up to 60% while the single-ended structure provides the power savings up to 69%, as compared to conventional flip-flops. Peiyi Zhao, Tarek K. Darwish has been worked on High-Performance and Low-Power Conditional Discharge (CDFF) Flip-Flop [5] in May 2004. In this paper, a modern conditional discharge flip-flop (CDFF) based on a conditional discharge technology is introduced. The offered CDFF not only reduces the internal switching activities of flip flops, but also generates less glitches at the output of flip flop, during maintaining the negative setup time and small to delay characteristics. With a data switching activity of 37%, the proposed conditional discharge flip flop can save up to 40% of the energy with the same speed that for the fastest pulsed flip-flops. Ying-Haw Shuu, Ming- Chang Sun, and Wu-Shhiung Feng, presents the paper XNOR-Based Double-Edge-Triggered Flip-Flop for Two-Phase Pipelines [6] in Feb 2006. In this paper a new designed DET-FF depending on an alternative XNOR gate is offered. Hamid Mahmmodi, Matthew Cooke, Vishy Tirumallashetty have proposed Ultra Low-Power Clocking Scheme Using Energy Recovery and Clock Gating [7]. This paper is introduced in Dec 2008. In this paper, four energy recovery clocked flip flops that are enable energy recovery from the clock network leading substantial energy savings, are introduced. The simulation results of the proposed flip-flop shows that a power reduces of 90% on the clock-tree and total power savings of up to 85% compared to the same implementation using the conventional square-wave clocking scheme and flip flops. Peiyi Zhaoo, and Zhoongfeng Wang worked on Design of Sequential Elements for Low Power Clocking System [8] in May 2011. With this proposed design the number of local clocked transistors can be effectively reduced to 40%. A 25% reduction of clock driving power has been attained. S.Esmaeilli, and Glenn E.R. Cowan workout A Low- Swing Differential Conditional Capturing Flip-Flop for LC Resonant Clock Distribution Networks [9] – This paper introduced in June 2012. Y.T. Hwang, J.F. Lin, and M.H. Sheu, go with Low power P-FF design with conditional pulse enhancement scheme [10] in Feb 2012. The maximum power saving of proposed FF is up to 40%. Majid Rahimi Nezhad, Mohsen Saneei presents the paper on Low-Power Pulsed Triggered Flip-Flop with New Explicit Pulse in 250-nm CMOS Technology [12]. Simulation outcomes of proposed flip-flop show that, for 50% data activity, power consumption is less than 7% to 30% lower than other flip-flops.

III. PROPOSED EXPLICIT P-FF DESIGN BASED ON A PASS TRANSISTOR

A. Conventional Explicit P-FF Designs

Generally implicit P-FFs are more power economical than explicit P-FF. Even so, they suffer from a longer discharging path inducing inferior timing characteristics. On the other hand, explicit pulse generation consumes more power than implicit pulse generation but the logic separation from the latch design establishes a unique speed advantage. Power consumption and the complexity of circuit of explicit flip-flop can be greatly brought down if one pulse generator is share a group of FFs (e.g., an *n*-bit register). In this paper, we are focusing explicit type P-FF designs only.

In this, we studied first some conventional explicit P-FF designs which are used as the reference designs in later performance comparisons.

1. EP-DCO- explicit Data closed to output Flip-Flop

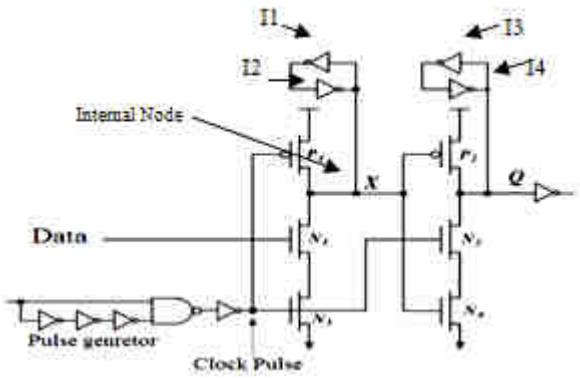

Fig.1: ep-DCO

Fig.1 shows data closed to output flip-flop design [7]. It consists of pulse generator of a three inverters connected to a NAND gate a semidynamic true-single-phase-clock (TSPC) structured latch design. In this explicit P-FF design,

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inverters I3 and I4 are used to latch data, and coupling circuit consisting inverters I1 and I2 used to hold the internal node *X*. Back-to-back end connected inverters i.e. I1 and I2 are act as a Keeper Logic. The delay of three inverters determines the pulse width of ep-DCO flip-flop. The serious drawback of ep-DCO P-FF is that in presence of static input '1', the internal node X is dropped off on every rising edge of the clock. This problem leads to large switching power dissipation. To get over this problem, some techniques such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed [4][7][9].

2. CDFF- conditional discharged flip-flop

Fig.2 shows a conditional discharged flip-flop design (CDFF) [4].To overcome the problem of continuous discharging of internal node X and large switching power dissipation in ep-DCO, CDFF is introduced.

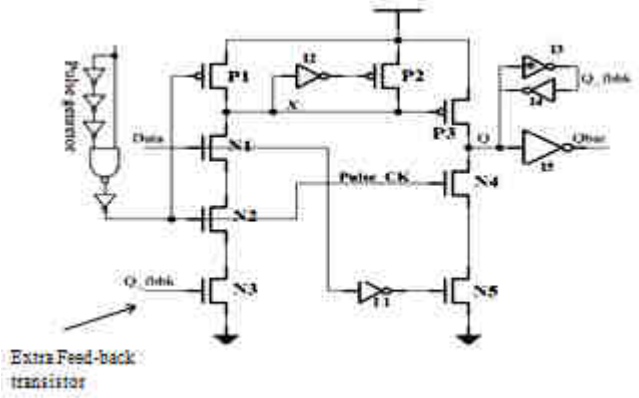

Fig.2: CDFF

In this, an extra n-MOS transistor MN3 controlled by the output signal Q-feedback is hired so that no discharge occurs at static input data "1." In addition, to simplify the circuit, the keeper logic at the internal node *X* is replaced with an inverter plus a pull-up p-MOS transistor only. But in CDFF, since discharging path consists of 3 stacked transistors MN1 to MN3, it face worst case delay. Therefore CDFF has longer data-to-Q (D-to-Q) delay.

3. MHLFF- modified hybrid latch flip-flop

Fig.3 shows modified hybrid latch flip-flop design. This is modified version of simple hybrid latch flip-flop. MHLFF uses static latch in which keeper logic at internal node X is removed. In this design, a weak pull-up transistor MP1 controlled by the output signal Q is used to maintain level of internal node X when Q equals to 0.

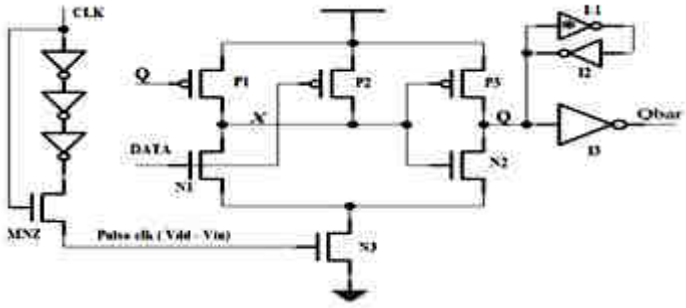

Fig.3: MHLFF

Though its circuitry is simple, it has two drawbacks. First one is it exhibits a longer D-to-Q delay during 0 to 1 transitions because node X is not pre-discharged. Another drawback of MHLFF is that node X becomes floating when output Q and input data both are equal to 1 and its value may drift causing excess DC power [6].

B. Proposed P-FF Design

Remembering the above four techniques, they all meet the same worst case timing occurring at 0 to 1 data transitions. The proposed design using a signal feed-through technique is introduced to improve this delay.

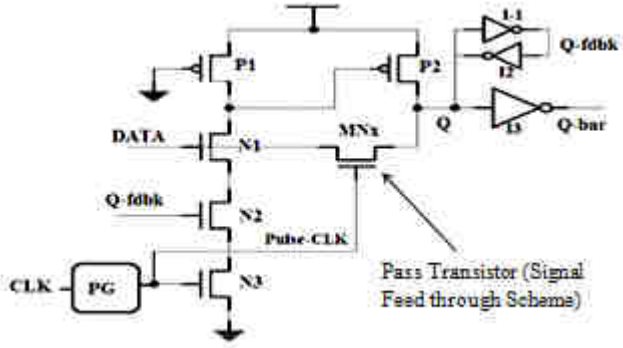

Fig.4: Proposed flip-flop

The proposed design acquires a static latch structure and a conditional discharge scheme to avoid surplus switching at an internal node X.

There are three major conflicts that makes the proposed design unique and distinct from the previous designs.

1. Addition of Pull-up pMOS transistor -

In proposed flip-flop, a weak pull-up pMOS transistor MP1 with gate connected to the ground is added in the first phase. This gives rise to a pseudo-nMOS logic style design. Pseudo nMOS transistor reduces number of devices and wiring complexity. The charge keeper circuit for the internal node can be saved due to the addition of pull-up pMOS transistor. With the circuit simplicity, this approach also keep down the load capacitance of node *X* [14], [15].

2. Pass Transistor MNx -

The extra component a pass transistor MNx controlled by the pulse clock is included in the proposed flip-flop design due to which input data can drive node Q of the latch

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directly (signal feed-through scheme). This pass transistor MNx provides a discharging path. The pass transistor MNx is thus played twofold role, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during "1" to "0" data transitions. Since input data can be drive directly to output through pass transistor, it reduces data transition delay.

3. Removal of Pull-down network –

Third, the pull-down network of the second stage inverter is completely removed in the proposed flip-flop design. Hence circuit complexity and layout area of proposed design is reduced. This proposed design actually improves the "0" to "1" delay and thus reduces the disparity between the rise time and the fall time delays.

In proposed design, when a clock pulse gets in, if no data transition occurs, i.e., the input data and node Q are at the same level, current passes through the pass transistor MNx, which keeps the input stage of the FF from any driving effort. At the same time, the input data and the output feedback Q_fdbk are complementary signal levels and the pull-down path of node *X* is off. Consequently, it leads in no signal switching occurs in any internal nodes. When a "0" to "1" data transition occurs, node *X* is discharged to turn on transistor MP2, which then pulls node Q high. With the signal feedthrough scheme, a boost can be obtained from the input source through the pass transistor MNx and the delay can be greatly sawed-off. When a "1" to "0" data transition occurs, transistor MNx is also turned on by the clock pulse and node Q is discharged by the input stage through this route. Unlike the case of "0" to "1" data transition, the input source bears the sole discharging responsibility. The loading effect to the input source is not significant because MNx is turned on for only a short time slot.

IV. SIMULATION RESULT

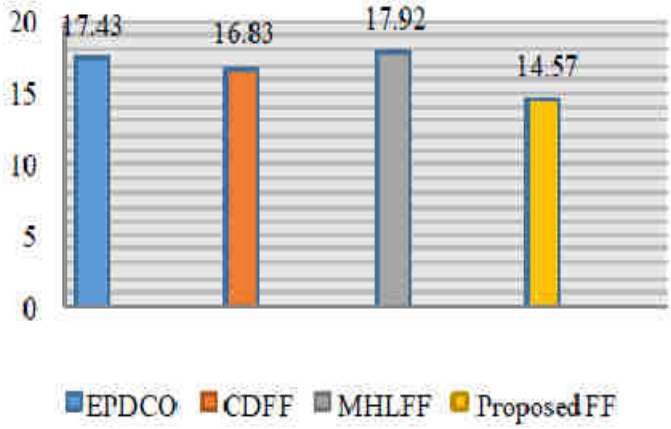
The performance of the proposed P-FF design is done through post-layout simulations. The proposed designs is compared with three explicit type P-FF designs. A conventional CMOS NAND-logic-based pulse generator design with a three-stage inverter chain is used for all P-FF designs except the MHLFF design, which employs its own pulse generation circuitry.

Table.1: Comparison Table

Type of Explicit Flip-Flop	Average power Dissipation (µW)	D-to-Q Delay (pSec)	No. of Transistors	Set-up Time (nSec)	Hold Time (nSec)
EPDCO	17.43	128.83	24	-0.0014	5
CDFF	16.83	121.32	26	10.13	20
MHLFF	17.92	156.30	19	0.167	10.1
Proposed FF	**14.57**	**111.67**	**20**	**0.10**	**0.131**

The target technology is the TSMC 180-nm CMOS process. Since pulse width design is essential to the correctness of data capture as well as the power consumption [10]–[13], the transistors of the pulse generator logic are sized for a design spec of 120 ps in pulse width in the TT case. The sizing also assures that the pulse generators can function properly in all process corners. With regard the latch structures, each P-FF design is individually optimized subject to the product of power and D-to-Q delay i.e. input to output delay. To mimic the signal rise and fall time delays, input signals are generated through buffers. Since the proposed design using signal feed through scheme requires direct output driving from the input source, for fair comparisons the power consumption of the data input buffer (an inverter) is included. The operating condition used in simulations is 500 MHz/1.8 V. The comparison is done regarding power consumption, delay, set-up time and hold time of the system.

A. Power Consumption of Flip-Flop Design



Graph.1: Average Power Calculation of Diff. Flip-Flop in Micro Watt

Since the proposed design uses less number of transistors, it has the smallest layout area. This is mainly because of the signal feed-through scheme, which largely reduces the transistor sizes on the discharging path. In terms of power behavior, the proposed design is the most efficient than the existing flip-flop designs. The given figure shows graphical representation of average power calculation of different flip-flops in microwatt.

B. Timing Parameters of Flip-Flop Design

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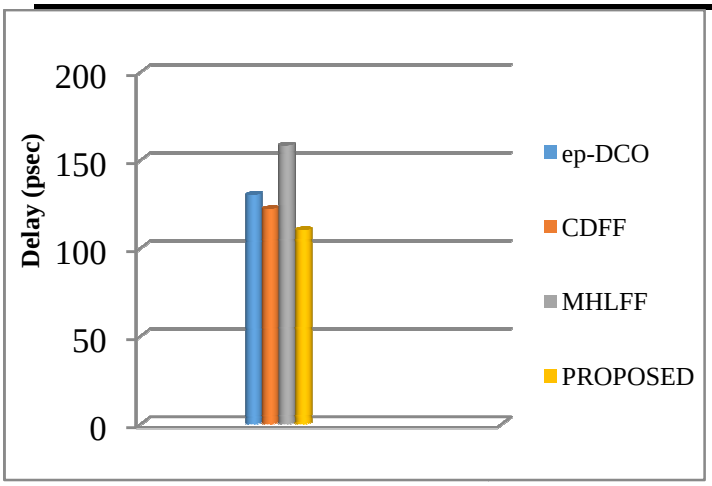

Graph.2: Delay Calculation of Diff. Flip-Flop in picoSec

After the analysis of power performances, we then examine the timing parameters of these FF designs. In order to function correctly, the edge triggered flip-flop requires the input to be stable for some time before the clock's active edge. This period is the set-up time. Given a sufficient setup time, the hold time is measured. Flip-flop design requires the state of the input to be held for some time after the clock edge. The time after the clock edge that the input has to remain stable is called hold time. In terms of set-up time and hold time, the proposed design is the most efficient than the existing flip-flop designs.

V. CONCLUSION

In this Paper, the several Flip flop designs like ep-DCO, CDFF, MHLLF & Proposed new P-FF are discussed. In this brief, we have presented a novel P-FF design by applying a modified TSPC latch structure integrating a mixed design significant style consisting of a pass transistor with p-seudo-nMOS logic. The key idea has been to provide a signal feed scheme through from input source to the internal node of the latch, which would be reduces the extra transition time and enhance both power and speed performance of flip flop. Extensive simulations have been conducted which supports the claim of the proposed design in various performance aspects. Simulation results indicate that proposed flip-flop design improves power performance and significantly reduces D to Q delay, set-up time and hold time.

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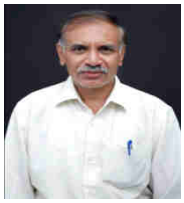

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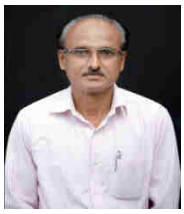

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